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4 Bit Flash ADC Configuration Utilizing TMCC and NOR ROM Encoder Using 180nm CMOS Technology

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***Abstract*— The paper designed is a 4-bit Flash Analog to Digital converter (ADC) with the use of Threshold modified comparator circuit (TMCC), used for voltage comparison and NOR ROM encoder with the use of 180nm Complementary Metal Oxide Semiconductor (CMOS) Technology by using cadence tool. Here TMCC's are introduced instead of conventional comparators. TMCC's compares very small voltages. It in-turn eliminates the complete resistor ladder and it improves the linearity as well in ADC. The clock rate used here is of 2 MHz and the voltage of operation is 1.8 V.**

***Index Terms*— ADC, TMCC, NOR ROM Encoder, Threshold voltage, Flash ADC, CMOS, Comparator.**

I. INTRODUCTION

ADC's are the very important part of any devices in the real world. ADC's are used to convert the analog signals (physical quantity) to digital signals (digital no.) , represents the amplitude of respective quantity. The performance of an ADC mainly depends on sampling rate, resolution as well as the power consumption. When we go with the power constraints, we prefer analog circuits. The power devoured by Digital CMOS rationale is conversely corresponding to square reverse of Scaling element (k).

i.e Digital Power $\alpha\ k^{-2}$

Whereas, analog power of CMOS is inversely proportional to scaling factor, keeping bandwidth constant.

i.e Analog Power $\alpha\ k^{-1}$

To reduce the complexity, the extreme use of digital logic has been taken place. The comparators which are used in the design are arranged parallel, so the better choice is Flash ADC because of its operational speed. The conventional Flash ADC is depicted in Fig.1. The resistors connected in series works as a voltage divider network, consuming large static power. Resolution and the number of used components are directly proportional to each other. The main constraints which we are interested in are area, speed and power. We have many techniques to save the power, they are folding, interpolating, bisection, inverter based comparator etc.

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A. Folding technique

For reducing the number of functional blocks, Folding technique is used. It is a transformation technique where unit-time processing to N-times processing takes place, N is folding factor. This technique requires more memory for data storage.

B. Interpolating technique

This technique reduces the number of pre-amplifiers (comparators). The requirement of latches remains the same. It is power efficient whereas requires more area.

C. Bisection technique

For every clock cycle, one-half of the comparators will work. It has capacity to reduce the power consumption by 43.18% . So the power consumption is less. The conversion speed is less.

D. Inverter based comparator

In the CMOS Inverter constitutes a PMOS and a NMOS transistor, by keeping the length constant, different threshold voltages can be calculated. In an inverter based comparator, two cascaded inverters are used to achieve high speed and lessen the power consumption.

In the traditional kind of Flash ADC, more power is devoured by the resistive step and the comparators. We can lessen the power utilization by decreasing the comparator tally. This paper primarily focuses on the plan of fast, an effective comparator (TMCC) and an encoder (NOR ROM sort) in CMOS innovation. Here it portrays the inside pieces like TMCC, 1 out of 15 encoder and NOR ROM encoder. In the following segment it exhibits the last execution of Flash ADC, then it is about reproduction comes about, at long last the conclusion.

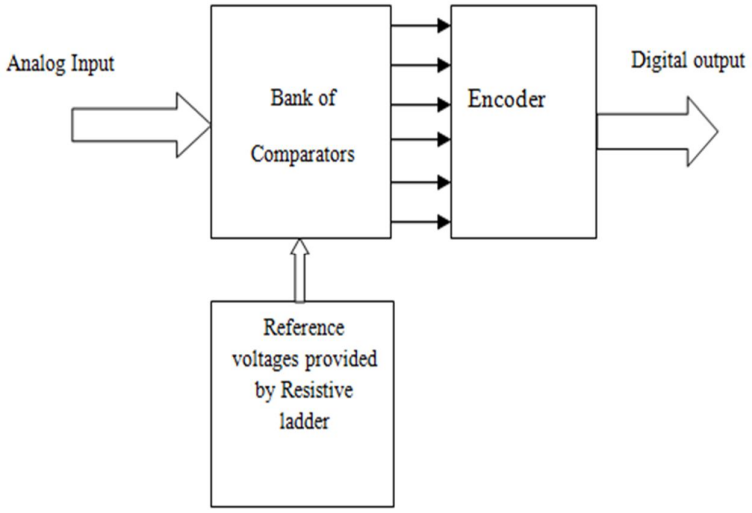

Figure 1. Conventional Flash ADC - Block Diagram

II. FLASH ADC AND ITS INTERNAL BLOCKS

The Flash ADC composed by the utilization of TMCC's, 1 out of N encoder and NOR ROM encoder as appeared in Fig.2. Fundamentally TMCC's are Buffer circuits, where in which their yields will be thermometer codes. They are encouraged to the 1 out of 15 encoder to keep any of the yield high around then. At that point that yield is encouraged to the NOR ROM encoder to get the twofold values (Digital output) .

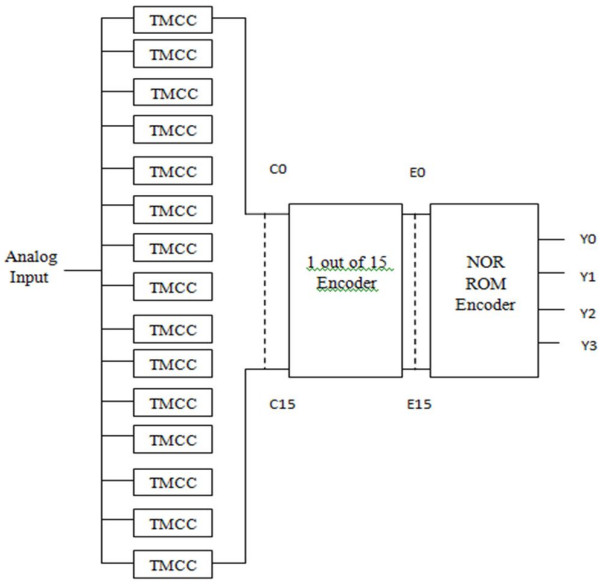

Figure 2. 4-Bit Flash ADC - Block Diagram

A. TMCC

Flash ADC is engineering's alternative, yet there will be loss (Intrinsic loss) in the resistor stepping stool circuit. TMCC's are fundamentally the circuits, comprises of an inverter with adjusted threshold voltage which is trailed by a NOT entryway as appeared in Fig.3. TMCC's thusly lessens the delay and the power utilization.

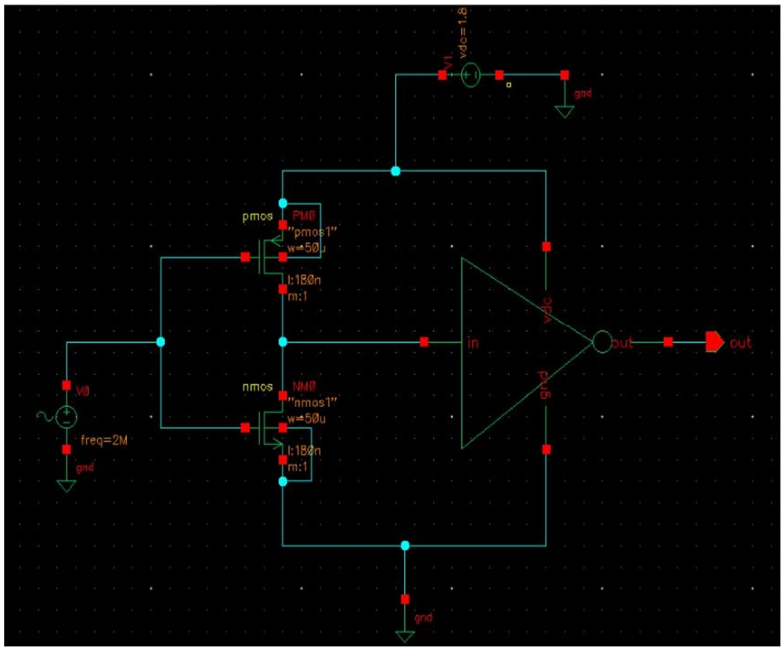

Figure 3. Schematic Of TMCC

Some of the equations for calculating the threshold voltage and the aspect ratio are as shown below:

$$V_{th} = \frac{V_{to,n} + \sqrt{\frac{1}{K_r}(V_{dd} + V_{to,p})}}{(1 + \frac{1}{\sqrt{K_r}})} \quad (1)$$

Where,

$$K_n = \mu_n C_{ox} (\frac{W}{L})_n \quad (2)$$

$$K_p = \mu_p C_{ox} (\frac{W}{L})_p \quad (3)$$

Transconductance ratio is given by,

$$K_r = \frac{K_n}{K_p} \quad (4)$$

$$\mu_n (\frac{W}{L})$$

The threshold voltage for each TMCC can be computed by changing the length and width of NMOS and PMOS individually. The table below depicts the different threshold values for different values of length and width.

TABLE 1. DIFFERENT THRESHOLD VOLTAGES OF TMCC

SN	TMCC	Vt (volt)	Wn(um)	Ln(um)	Wp(um)	Lp(um)
1	1st	0.3	50	0.18	0.45	0.18
2	2nd	0.4	30	0.18	1	0.18
3	3rd	0.5	30	0.18	5	0.18
4	4th	0.559	25	0.18	5	0.18
5	5th	0.688	10	0.18	5	0.18
6	6th	0.802	20	0.18	30	0.18
7	7th	0.834	10	0.18	15	0.18
8	8th	1.008	5	0.18	25	0.18
9	9th	1.037	2	0.18	18	0.18
10	10th	1.048	5	0.18	35	0.18
11	11th	1.069	2	0.18	20	0.18
12	12th	1.13	2	0.18	38	0.18
13	13th	1.152	2	0.18	50	0.18
14	14th	1.2	0.4	0.18	40	0.18
15	15th	1.235	1	0.18	50	0.18

At the point when the input voltage not as much as that of threshold voltage , PMOS is ON, NMOS is OFF, which gives high yield i.e Logic 1. At the point when the input voltage exceeds threshold voltage , NMOS is ON, results in low yield i.e Logic 0. TMCC performs opposite to that of a normal comparator. The benefit of adding a not gate is for logical restoration of the output. The TMCC transient response is depicted in Fig.4. The TMCC DC Response is depicted in Fig.5 The TMCC bank DC Response is depicted in Fig.6.

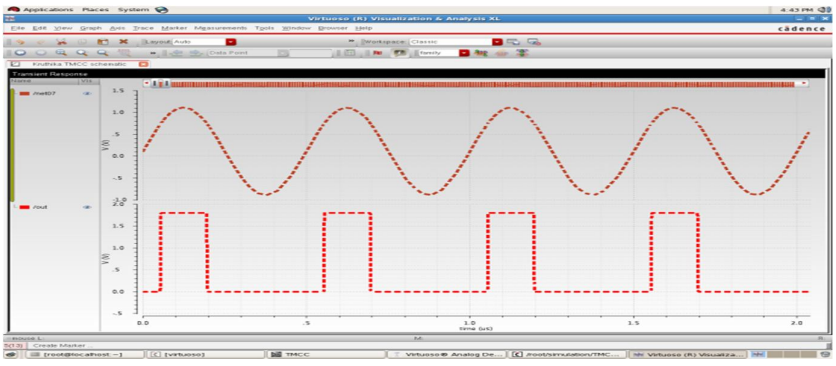

Figure 4. TMCC - Transient Response

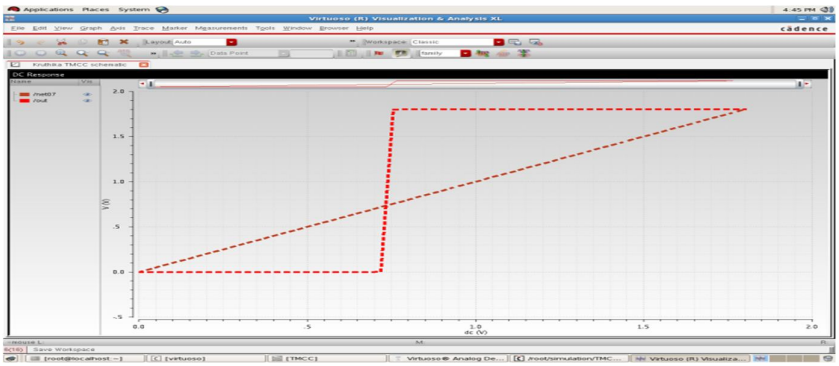

Figure.5. Tmcc - Dc Response

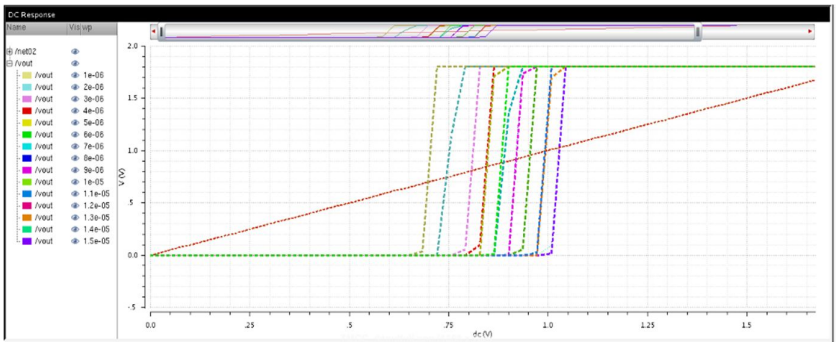

Figure 6. TMCC Bank - DC Response

B. 1 Out of 15 Encoder

The schematic of 1 out of 15 Encoder is as depicted in Fig.7.Interpretation of thermometer code from the comparator yield to double code through the encoder is critical thing in an ADC. It constitutes AND entryway and NOT door. The NOR ROM Encoder information is the yield from the AND entryway. The 1 out of 15 encoder block diagram is as depicted in Fig 8.

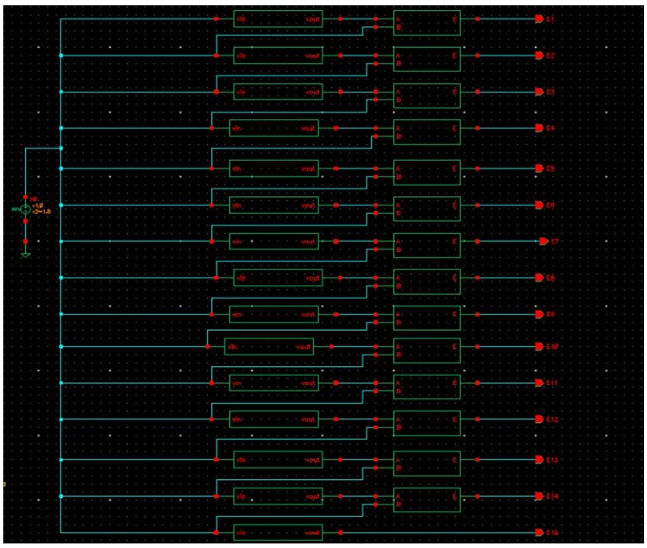

Figure 7. Schematic of 1 out of 15 encoder

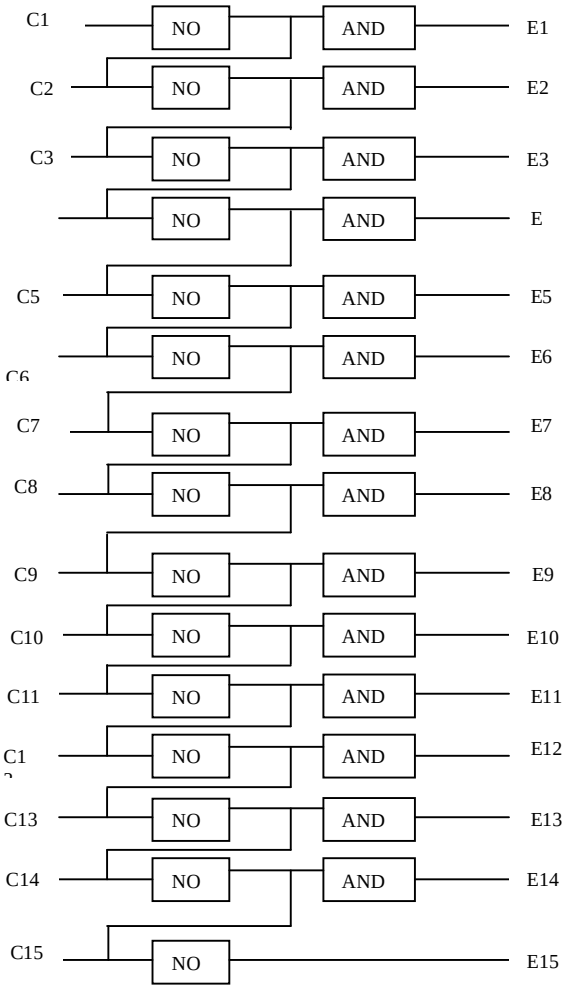

Figure 8. 1 out of 15 Encoder - Block diagram

It is the mix of NOT entryway AND door. The blend is done such that atleast one of the yield will be high around then. It has 15 Inverters and 14 AND entryways. The DC response of 1 out of 15 Encoder is depicted below in Fig.9.

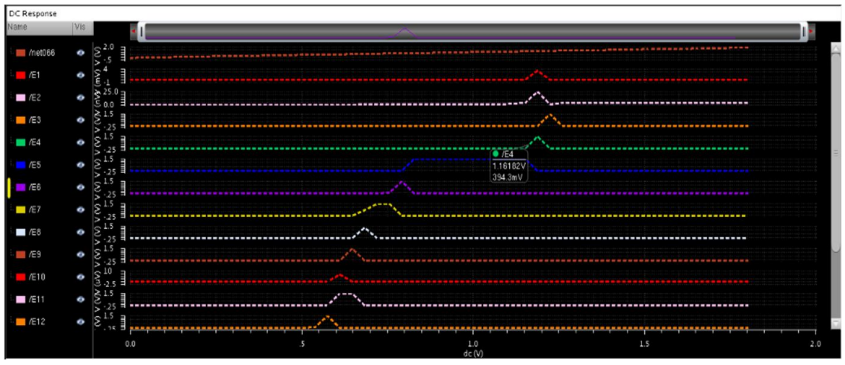

Figure 9. 1 out of 15 Encoder - DC response

C. NOR ROM Encoder

The comparator output will be in the encoded form. The conversion of encoded signal into binary code can be done by designing on encoder. This is done with the use of ROM type encoder schematic as depicted in Fig.10.

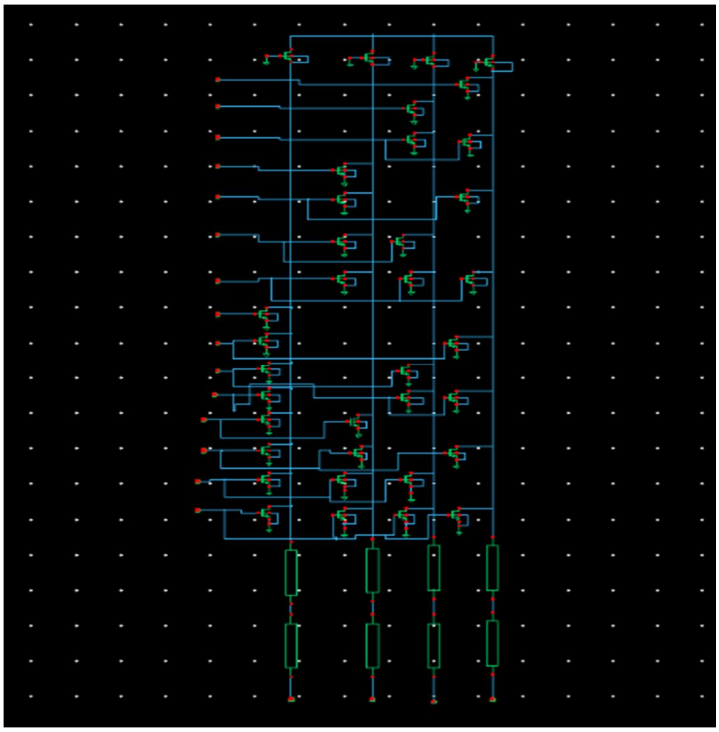

Figure.10. Nor Rom Encoder – Schematic

III. IMPLEMENTATION: FLASH TYPE ADC

The Flash type ADC schematic is as appeared in Fig.11. It comprises of TMCC's, 1 out of 15 Encoder with NOR ROM sort encoder by utilizing cadence tool in CMOS innovation. Analog input will be contrasted and 15 diverse TMCC's reference voltages, after which they are changed over into computerized frame with the utilization of 1 out of 15 encoder and NOR ROM sort of encoder. In this manner the analog signal is in turn changed over into computerized frame by utilizing Flash type ADC.

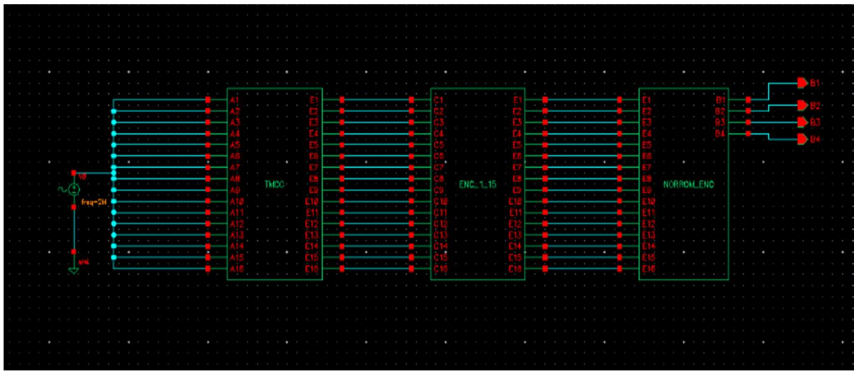

Figure.11. Flash Adc – Schematic

IV. RESULTS

The Flash ADC configuration utilizes 15 TMCC's, 1 out of 15 Encoder and a NOR ROM Encoder. ADC produces yield of 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011,1100, 1101, 1110, 1111. Here we utilize 1.8v, so we partition 1.8v into a few voltages, each will be of 0.1125v. Fig 12 portrays Transient Response of Flash ADC with clock rate of 2 MHz. At the point when the info voltage is 0.1125v, ADC will create 0001 et cetera. Along these lines the info simple voltage is changed over to Digital frame.

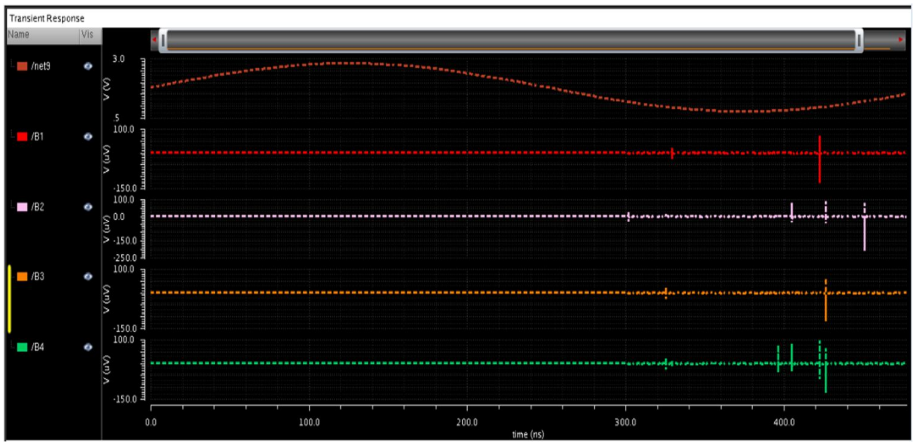

Figure 12. 4 Bit Flash Adc - Transient Response

V. CONCLUSION

The plan of 4 bit Flash ADC is done utilizing 180nm CMOS innovation. The advantages of this design is, devours less power since resistor stepping stool is totally wiped out. The clock rate of 2 MHz is utilized. TMCC decreases the coordinating issue by giving the fast. TMCC configuration requires just 4 transistors, so requires less power and lesser chip range.

VI. ACKNOWLEDGEMENT

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REFERENCES

[1] K. N. Hosur *et al.*, "Design of 4 bit flash ADC using TMCC & NOR ROM encoder in 90nm CMOS technology," *2015 International Conference on Trends in Automation, Communications and Computing Technology (I-TACT-15)*, Bangalore, 2015, pp. 1-6.

[2] A. Kar, A. Majumder, A. J. Mondal and N. Mishra, "Design of ultra low power flash ADC using TMCC & bit referenced encoder in 180nm technology," *2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA)*, Bangalore, 2015, pp. 1-6.

[3] Megha R and Pradeepkumar K A, "Implementation of low power flash ADC by reducing comparators," *2014 International Conference on Communication and Signal Processing*, Melmaruvathur, 2014, pp. 443-447.

[4] I. S. A. Halim, S. L. M. Hassan, N. D. b. M. Akbar and A. A. A. Rahim, "Comparative study of comparator and encoder in a 4-bit Flash ADC using 0.18µm CMOS technology," *2012 International Symposium on Computer Applications and Industrial Electronics (ISCAIE)*, Kota Kinabalu, 2012, pp. 35-38.

[5] Sudakar S. Chauhan, S. Manabala, S.C. Bose, and R. Chandel, "A New Approach To Design Low Power CMOS Flash A/D Converter", International Journal of VLSI design & Communication Systems VLSICS),Vol.2, No.2, June 2011.

[6] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design, Second Edition", Oxford University Press.

[7] S. Sheikhaei, S. Mirabbasi and A. Ivanov, "A 43 mW single-channel 4GS/s 4-bit flash ADC in 0.18 µm CMOS," *2007 IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2007, pp. 333-336.

[8] R.Jacob Baker, Harry W.Li and David E.Boyce , “CMOS CIRCUIT DESIGN, LAYOUT AND SIMULATION “, IEEE press series on Microelectronic systems Stuart K Tewksbury, series editor.

[9] Prof. S.S. Khot, Dr. P. W. Wani, Dr M S Sutaone, Shubhang Tripathi “Design of a 45nm TIQ Comparator for High Speed and Low Power 4-Bit Flash ADC”, ACEEE Int. J. on Electrical and Power Engineering, Vol. 02, No. 01, Feb 2011.

[10] M. Das, B. Nath, D. Sarkar, A. Kar and A. Majumder, "Design of ultra low power novel 3-bit flash ADC in 45nm CMOS technology," *2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM)*, Chennai, 2015, pp. 239-244.